SSI INTERFACE

GENERAL DESCRIPTION

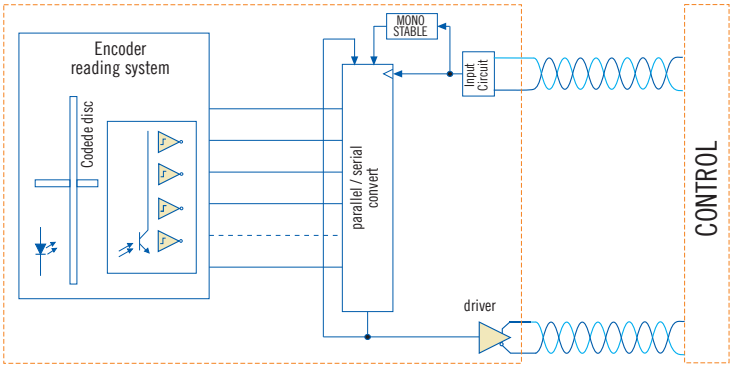
ISO 9001:2000

INTRODUCTION

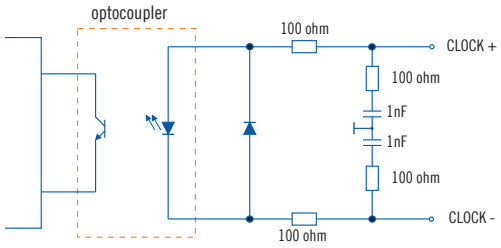
Evolution in automation is continuously growing and so its request for precision in measurement devices and consequentially also in absolute encoder. To satisfy these demands, absolute encoders have been designed with higher and higher resolutions. However, higher precision means an increasing number of bits and consequently a growing need of wires. SSI interface was created in order to contain installation costs and to simplify wiring. This interface transmits data in a serial mode by using only two signals (CLOCK and DATA), independently from the precision of the encoder.

DESCRIPTION

The SSI interface allows the transmission of the absolute encoder position data by a serial line synchronized by a clock. The following figure shows the block diagram of an encoder featuring an SSI interface:



The working principle of an encoder with an SSI interface is very similar to a standard one. Main parts are: a light source, a disc with transparent and opaque windows, photo-electric receivers, comparison/trigger circuits, a parallel/serial converter, a mono-stable circuit, an input circuit for the clock signal and an output driver for the data signal.
The position data is obtained by the encoder reading system and continuously transmitted to a parallel/serial converter (based by a "shift register" with parallel loading). When the mono-stable circuit is activated by a clock signal transition, the data is stored and transmitted to the output synchronized with the clock signal. CLOCK and DATA signals are transmitted differentially (RS422) to enhance immunity from interference and to allow longer transmission distances.



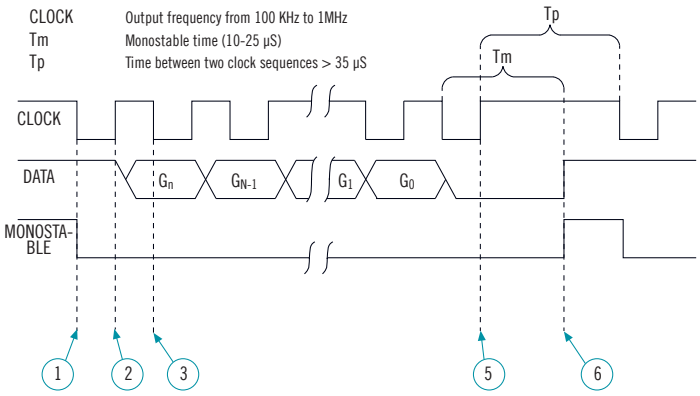
CLOCK signal circuit input

DATA signal circuit output

WORKING PRINCIPLE

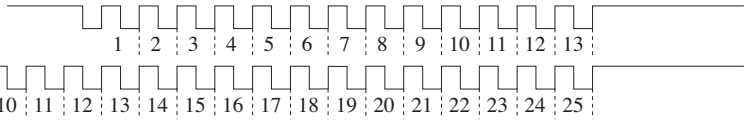
When quiescent, CLOCK and DATA signals have a high logical status and the mono-stable circuit is disabled.

1. On the first CLOCK signal descent front, the mono-stable is activated and the parallel value at the P/S converter input is stored into the shift register.
2. On the CLOCK signal ascent front, the Most Significant Bit (MSB) is copied into the DATA signal output.
3. On the CLOCK descent front (when the signal is stable) the controller acquires the level value from the DATA signal and the mono-stable is re-activated.
4. On each further ascent front of the CLOCK pulse sequence, following bits up to the least significant one are copied in the DATA signal output and then acquired by the control on the descent front.
5. At the end of the CLOCK pulse sequence, when the external control has also acquired the value of the Least Significant Bit (LSB), the CLOCK pulse sequence stops and
therefore the mono-stable is no longer re-activated.
6. Once the mono-stable time (Tm) has elapsed, the DATA signal returns to a high logical status and the mono-stable disables itself.



TRANSMISSION PROTOCOL

The frame length of the transmitted data depends only on the encoder type (singleturn or multiturn) and not on the resolution. In fact, the standard frame length for a singleturn encoder is 13 bits, whilst for a multiturn one it is 25 bit. The MSB is in the center of the data, as shown by the below reported table:



T	2^T																												Ta		2^n	n
12	4096	1	1	G_{n+11}	G_{n+10}	G_{n+9}	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	G_{n-11}	G_{n-12}	G_{n-13}	0	1	8192	13
11	2048	1	1	0	G_{n+10}	G_{n+9}	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	G_{n-11}	0	0	0	1	4096	12
10	1024	1	1	0	0	G_{n+9}	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	0	0	0	0	1	2048	11
9	512	1	1	0	0	0	G_{n+8}	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	G_{n-10}	0	0	0	0	1	1024	10
8	256	1	1	0	0	0	0	G_{n+7}	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	G_{n-9}	0	0	0	0	0	1	512	9
7	128	1	1	0	0	0	0	0	G_{n+6}	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	G_{n-8}	0	0	0	0	0	0	1	256	8
6	64	1	1	0	0	0	0	0	0	G_{n+5}	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	G_{n-7}	0	0	0	0	0	0	0	1	128	7
5	32	1	1	0	0	0	0	0	0	0	G_{n+4}	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	G_{n-6}	0	0	0	0	0	0	0	0	1	64	6
4	16	1	1	0	0	0	0	0	0	0	0	G_{n+3}	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	G_{n-5}	0	0	0	0	0	0	0	0	0	1	32	5
3	8	1	1	0	0	0	0	0	0	0	0	0	G_{n+2}	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	G_{n-4}	0	0	0	0	0	0	0	0	0	0	1	16	4
2	4	1	1	0	0	0	0	0	0	0	0	0	0	G_{n+1}	G_n	G_{n-1}	G_{n-2}	G_{n-3}	0	0	0	0	0	0	0	0	0	0	0	1	8	3
1	2	1	1	0	0	0	0	0	0	0	0	0	0	0	G_n	G_{n-1}	G_{n-2}	0	0	0	0	0	0	0	0	0	0	0	0	1	4	2

singleturn

multiturn

Number of turn

PPR

The transmitted frame format depends on the bit per turn and bit for turns encoder configuration.

n = number of bits per revolution

T = number of bits for turns

Ta = $Tm - \frac{Tc}{2}$

Tc = clock period

Tm = monoflop time

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